

Distributed Gate Thyristor Type SA12LP0472EE

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SA	12	LP	0472	E	E	
-	Voltage Code	Outline Code	Current code	Type code	t_q code	Optional code
t _q code: E = 25 μ s, F = 30 μ s						

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Absolute Maximum Ratings

VOLTAGE RATINGS		MAXIMUM LIMITS	UNITS
V_{DRM}	Repetitive peak off-state voltage, (note 1)	1200	V
V_{DSM}	Non-repetitive peak off-state voltage, (note 1)	1200	V
V_{DDC}	Maximum DC of-state voltage, (note 1)	810	V
V_{RRM}	Repetitive peak reverse voltage, (note 1)	1200	V
V_{RSM}	Non-repetitive peak reverse voltage, (note 1)	1300	V
V_{RDC}	Maximum DC reverse voltage, (note 1)	810	V
note 1)	De-rating factor of 0.13%/°C is applicable for T_j below 25°C		

OTHER RATINGS		MAXIMUM LIMITS	UNITS
$I_{T(AV)M}$	Maximum average on-state current, $T_{sink} = 55^\circ\text{C}$, (note 1)	472	A
$I_{T(AV)M}$	Maximum average on-state current, $T_{sink} = 85^\circ\text{C}$, (note 1)	316	A
$I_{T(AV)M}$	Maximum average on-state current, $T_{sink} = 85^\circ\text{C}$, (note 2)	185	A
$I_{T(RMS)}$	Nominal RMS on-state current, $T_{sink} = 25^\circ\text{C}$ (note 1)	945	A
$I_{T(d.c.)}$	D.C. on-state current, $T_{sink} = 25^\circ\text{C}$, (note 3)	789	A
I_{TSM}	Peak non-repetitive surge current $t_p = 10\text{ms}$, $V_{RM} = 60\%V_{RRM}$, (note4)	4.3	kA
I_{TSM2}	Peak non-repetitive surge current $t_p = 10\text{ms}$, $V_{RM} \leq 10\text{V}$, (note 4)	4.7	kA
I^2t	I^2t capacity for fusing $t_p = 10\text{ms}$, $V_{RM} = 60\%V_{RRM}$, (note 4)	$92.5 \cdot 10^3$	A^2s
I^2t	I^2t capacity for fusing $t_p = 10\text{ms}$, $V_{RM} \leq 10\text{V}$, (note 4)	$110.5 \cdot 10^3$	A^2s
$(di/dt)_{cr}$	Critical rate of rise of on-state current (repetitive), (note 5)	500	$\text{A}/\mu\text{s}$
	Critical rate of rise of on-state current (non repetitive), (note 5)	1000	$\text{A}/\mu\text{s}$
V_{RGM}	Peak reverse gate voltage	5	V
$P_{G(AV)}$	Mean forward gate power	2	W
P_{GM}	Peak forward gate power	30	W
T_{jop}	Operating temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-40 to +150	°C
note 1)	Double-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 2)	Single-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 3)	Double-side cooled		
note 4)	Half-sinewave, 125°C T_j initial		
note 5)	$V_D = 67\%V_{DRM}$, $I_{FG} = 2\text{A}$, $t_R \leq 0.5\mu\text{s}$, $T_{case} = 125^\circ\text{C}$		

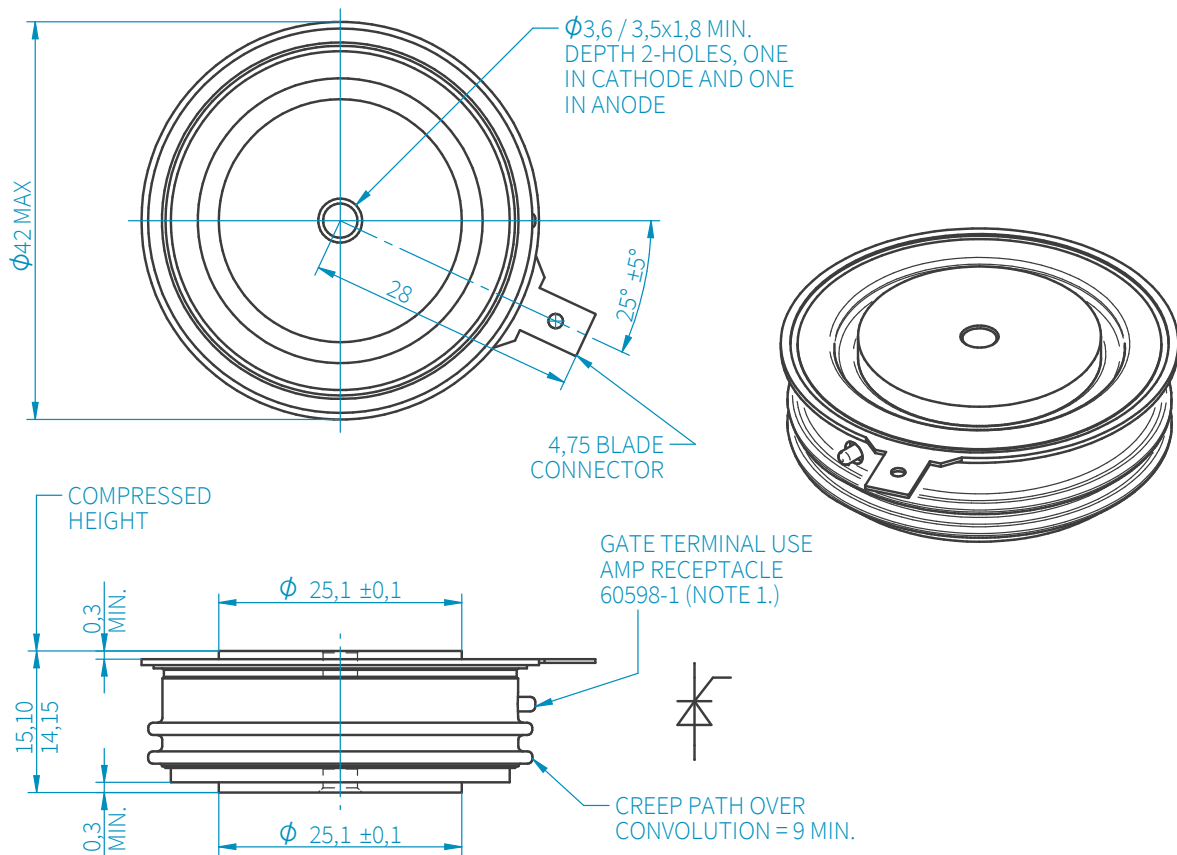
Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
V _{TM}	Maximum peak on-state voltage	I _{TM} = 1000A	-	-	2.80 V	
		I _{TM} = 1416A	-	-	3.24 V	
V _{T0}	Threshold voltage	-	-	1.648	V	
r _T	Slope resistance	-	-	1.125	mΩ	
(dv/dt) _{CR}	Critical rate of rise of off-state voltage	V _D = 80%V _{DRM} , Linear ramp, Gate o/c	200	-	-	V/μs
I _{DRM}	Peak off-state current	Rated V _{DRM}	-	-	60	mA
I _{RRM}	Peak reverse current	Rated V _{RRM}	-	-	60	mA
V _{GT}	Gate trigger voltage	T _j = 25°C, V _D = 10V, I _T = 3A	-	-	3.0	V
I _{GT}	Gate trigger current		-	-	200	mA
V _{GD}	Gate non-trigger voltage	Rated V _{DRM}	-	-	0.25	V
I _H	Holding current	T _j = 25°C	-	-	1000	mA
t _{GD}	Gate controlled turn-on delay time	V _D = 67%V _{DRM} , I _{TM} = 2000A, di/dt = 60A/μs,	-	0.4	1.0	μs
t _{GT}	Turn-on time	I _{FG} = 2A, t _r = 0.5μs, T _j = 25°C	-	1.0	2.0	μs
Q _{RR}	Recovered charge		-	155	175	μC
Q _{RA}	Recovered charge, 50% Chord	I _{TM} = 550A, t _p = 500μs, di/dt = 40A/μs, V _R = 50V	-	70	-	μC
I _{RM}	Reverse recovery current		-	60	-	A
t _{RR}	Reverse recovery time		-	2.5	-	μs
t _{GQ}	Turn-off time (note 2)	I _{TM} = 550A, t _p = 500μs, di/dt = 40A/μs, V _R = 50V, V _{DR} = 80%V _{DRM} , dV _{DR} /dt = 20V/μs	-	20	25	μs
		I _{TM} = 550A, t _p = 500μs, di/dt = 40A/μs, V _R = 50V, V _{DR} = 80%V _{DRM} , dV _{DR} /dt = 200V/μs	-	25	30	μs
R _{thJK}	Thermal resistance, junction to sink (note 3)	Double-side cooled	-	-	0.05	K/W
		Single-side cooled	-	-	0.10	K/W
F	Mounting force	(note 3)	5	-	9	kN
W _t	Weight		-	90	-	g
note 1)	Unless otherwise indicated T _j = 125°C					
note 2)	The required t _Q (specified with dV _{DR} /dt = 200V/μs) is 25μs					
note 3)	For other clamp forces, please consult factory					

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