Distributed Gate Thyristor Type SA14AP1178EF

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Data Sheet Issue: 1

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SA	14	AP	1178	E	F	
-	Voltage Code	Outline Code	Current code	Type code	t_q code	Optional code
t_q code: E = 25µs, F = 30µs, G = 35µs						

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Absolute Maximum Ratings

	VOLTAGE RATINGS	MAXIMUM LIMITS	UNITS
V_{DRM}	Repetitive peak off-state voltage, (note 1)	1400	V
V_{DSM}	Non-repetitive peak off-state voltage, (note 1)	1400	V
V_{DDC}	Maximum DC of-state voltage, (note 1)	930	V
V_{RRM}	Repetitive peak reverse voltage, (note 1)	1400	V
V_{RSM}	Non-repetitive peak reverse voltage, (note 1)	1400	V
V_{RDC}	Maximum DC revrese voltage, (note 1)	930	V
note 1)	De-rating factor of 0.13%/°C is applicable for T_j below 25°C		

	OTHER RATINGS	MAXIMUM LIMITS	UNITS
$I_{T(AV)M}$	Maximum average on-state current, T_{sink} = 55°C, (note 1)	1178	A
$I_{T(AV)M}$	Maximum average on-state current, T_{sink} = 85°C, (note 1)	767	A
$I_{T(AV)M}$	Maximum average on-state current, T_{sink} = 85°C, (note 2)	433	A
$I_{T(RMS)}$	Nominal RMS on-state current, T_{sink} = 25°C (note 1)	2395	A
$I_{T(d.c.)}$	D.C. on-state current, T_{sink} = 25°C, (note 3)	1916	A
I_{TSM}	Peak non-repetitive surge current t_p = 10ms, V_{RM} = 60%V_{RRM}, (note4)	17.0	kA
I_{TSM2}	Peak non-repetitive surge current t_p = 10ms, $V_{RM} \leq$ 10V, (note 4)	18.7	kA
I^2t	I^2t capacity for fusing t_p = 10ms, V_{RM} = 60%V_{RRM}, (note 4)	$1.45 \cdot 10^6$	A^2s
I^2t	I^2t capacity for fusing t_p = 10ms, $V_{RM} \leq$ 10V, (note 4)	$1.75 \cdot 10^6$	A^2s
$(di/dt)_{cr}$	Critical rate of rise of on-state current (repetitive), (note 5)	1000	A/µs
	Critical rate of rise of on-state current (non repetitive), (note 5)	1500	A/µs
V_{RGM}	Peak reverse gate voltage	5	V
$P_{G(AV)}$	Mean forward gate power	2	W
P_{GM}	Peak forward gate power	30	W
V_{GD}	Non-trigger gate voltage, (note 6)	0.25	V
T_{jop}	Operating temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-40 to +150	°C
note 1)	Double-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 2)	Single-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 3)	Double-side cooled		
note 4)	Half-sinewave, 125°C T_j initial		
note 5)	V_D = 67%V_{DRM}, I_{FG} = 2A, $t_R \leq$ 0.5µs, T_{case} = 125°C		
note 6)	Rated V_{DRM}		

Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{TM}	Maximum peak on-state voltage	I_{TM} = 2000A	-	-	2.2	V
V_{T0}	Threshold voltage		-	-	1.6	V
r_T	Slope resistance		-	-	0.3	mΩ
$(dv/dt)_{CR}$	Critical rate of rise of off-state voltage	V_D = 80%V_{DRM}	200	-	-	V/µs
I_{DRM}	Peak off-state current	Rated V_{DRM}	-	-	150	mA
I_{RRM}	Peak reverse current	Rated V_{RRM}	-	-	150	mA
V_{GT}	Gate trigger voltage	T_j = 25°C, V_D = 10V, I_T = 2A	-	-	3.0	V
I_{GT}	Gate trigger current		-	-	300	mA
I_H	Holding current	T_j = 25°C	-	-	1000	mA
t_{GD}	Gate controlled turn-on delay time	V_D = 67%V_{DRM}, I_{TM} = 2000A, di/dt = 60A/µs, I_{FG} = 2A, t_r = 0.5µs, T_j = 25°C	-	0.4	1.2	µs
t_{GT}	Turn-on time		-	1.0	3.0	µs
Q_{RR}	Recovered charge	I_{TM} = 1000A, t_p = 1000µs,di/dt = 60A/µs, V_R = 50V	-	-	350	µC
Q_{RA}	Recovered charge, 50% Chord		-	170	190	µC
I_{RM}	Reverse recovery current		-	-	130	A
t_{RR}	Reverse recovery time		-	-	3.7	µs
t_{GQ}	Turn-off time (note 2)	I_{TM} = 1000A, t_p = 1000µs, di/dt = 60A/µs, V_R = 50V, V_{DR} = 80%V_{DRM}, dV_{DR}/dt = 20V/µs	-	-	35	µs
		I_{TM} = 1000A, t_p = 1000µs, di/dt = 60A/µs, V_R = 50V, V_{DR} = 80%V_{DRM}, dV_{DR}/dt = 200V/µs	25	-	35	µs
R_{thJK}	Thermal resistance, junction to sink (note 3)	Double-side cooled	-	-	0.024	K/W
		Single-side cooled	-	-	0.048	K/W
F	Mounting force	(note 3)	19	-	26	kN
W_t	Weight		-	340	-	g
note 1)	Unless otherwise indicated T_j = 125°C					
note 2)	The required t_Q (specified with dV_{DR}/dt = 200V/µs) is 30µs					
note 3)	For other clamp forces, please consult factory					

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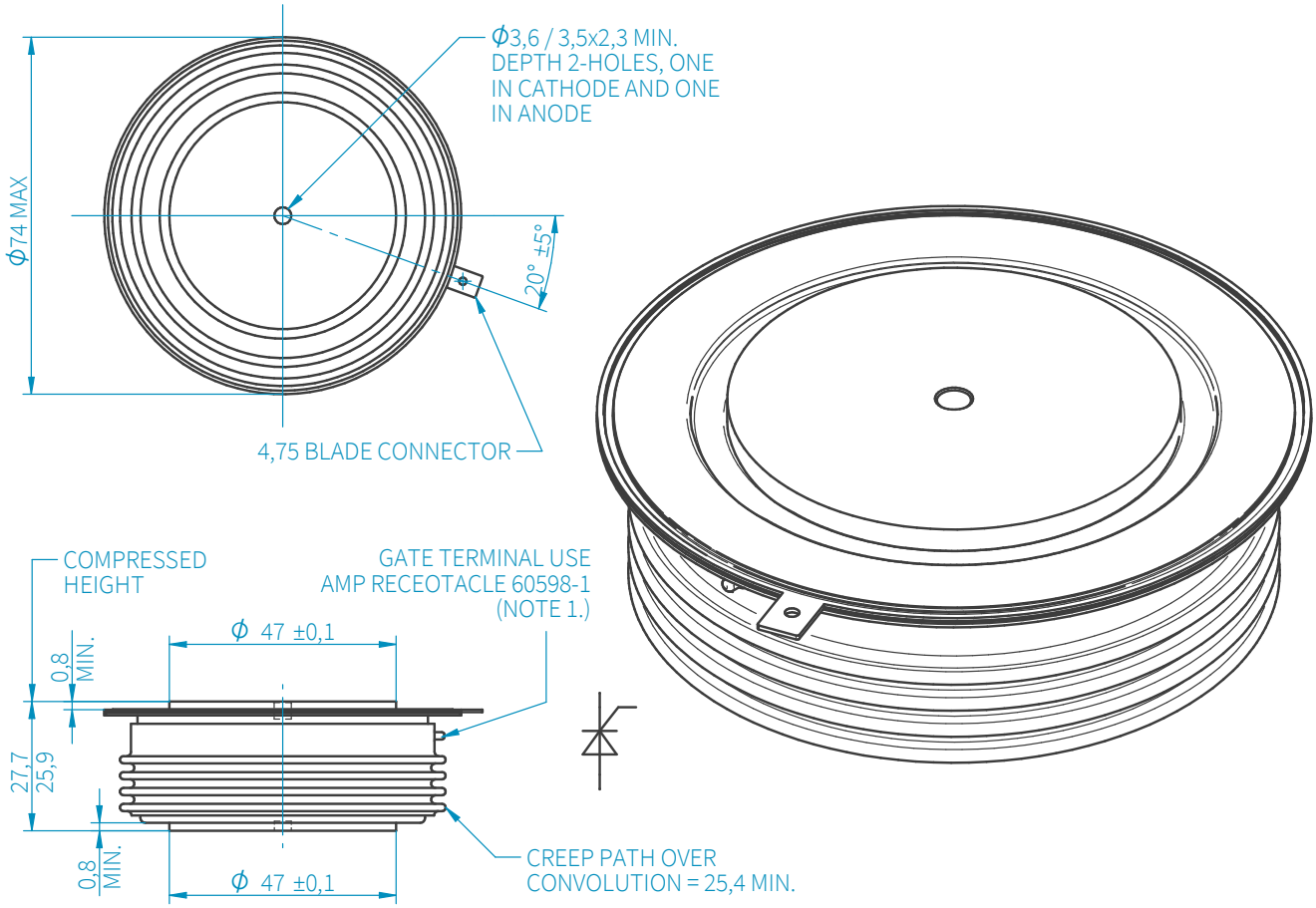
Outline Drawing



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