Symmetrical Gate Turn-Off Thyristor Type SA14XP0700F0

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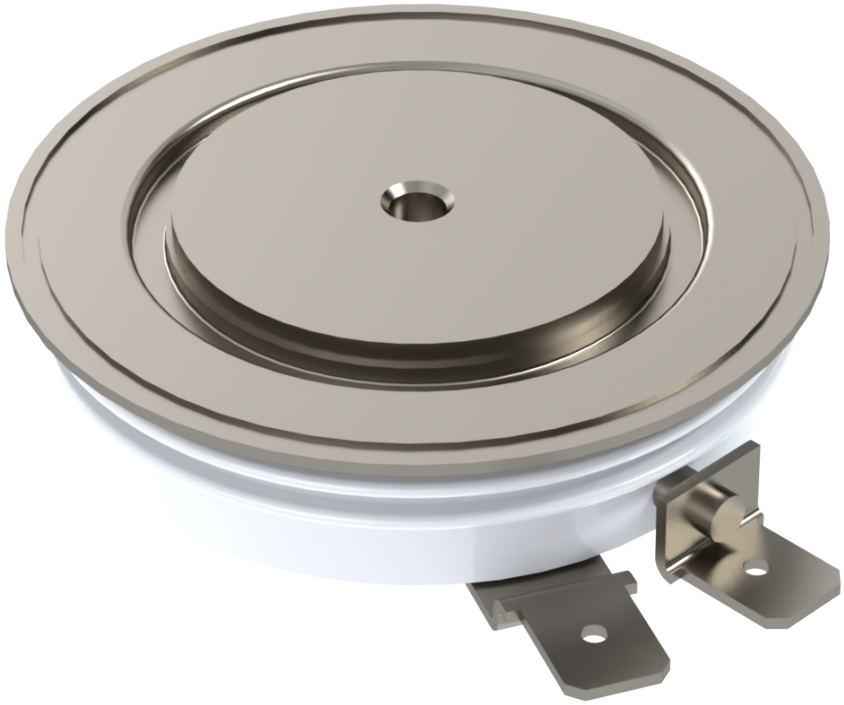

ORDERING INFORMATION						(Please quote 12 to 15 digit code as below)
SA	14	XP	0700	F	0	
-	Voltage Code	Outline Code	Current code	Type code	Special code	Optional code

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Absolute Maximum Ratings

	VOLTAGE RATINGS	MAXIMUM LIMITS	UNITS
V_{DRM}	Repetitive peak off-state voltage, (note 1)	1400	V
V_{RSM}	Non-repetitive peak off-state voltage, (note 1)	1500	V
V_{RRM}	Repetitive peak reverse voltage	1400	V
V_{RSM}	Non-repetitive peak reverse voltage	1400	V
note 1)	V_{GK} = –2V		

	OTHER RATINGS	MAXIMUM LIMITS	UNITS
I_{TGQ}	Peak turn-off current (note 1)	700	A
L_S	Snubber loop impedance, $I_{TM} = I_{TGQ}$ (note 1)	0.3	nH
$I_{T(AV)M}$	Mean on-state current, T_{sink} = 55°C, (note 2)	430	A
$I_{T(RMS)}$	Nominal RMS on-state current, T_{sink} = 25°C (note 2)	870	A
I_{TSM}	Peak non-repetitive surge current t_p = 10ms	5	kA
I_{TSM2}	Peak non-repetitive surge current t_p = 2ms (note 3)	9	kA
I^2t	I^2t capacity for fusing t_p = 10ms	$125 \cdot 10^3$	A^2s
$(di/dt)_{cr}$	Critical rate of rise of on-state current, (note 4)	1000	A/µs
P_{FGM}	Peak forward gate power	160	W
P_{RGM}	Peark reverse gate power	5	kW
I_{FGM}	Peak forward gate current	100	A
V_{RGM}	Peak reverse gate voltage (note 5)	18	V
t_{off}	Minimum permissible off-time, $I_{TM} = I_{TGQ}$ (note 1)	70	µs
t_{on}	Minimum permissible off-time	20	µs
T_{jop}	Operating temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-40 to +150	°C
note 1)	T_j = 125°C, V_D = 80%V_{DM}, $V_{DM} \leq V_{DRM}$, di_{GQ}/dt = 20A/µs, $I_{TM} = I_{TGQ}$ and C_S = 1.5µF		
note 2)	Double-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 3)	Half-sinewave, t_p = 2ms		
note 4)	For di/dt > 1000A/µs please consult factory.		
note 5)	May exceed this value during turn-off avalanche period.		

Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{TM}	Maximum peak on-state voltage	I_G = 1.5A, I_T = 700A	-	1.9	2.2	V
I_L	Latching current	T_j = 25°C	-	5	-	A
I_H	Holding current		-	5	-	A
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage	V_D = 80%V_{DRM}, V_{GR} = –2V	800	-	-	V/µs
I_{DRM}	Peak off-state current	Rated V_{DRM}, V_{GR} = –2V	-	-	30	mA
I_{RRM}	Peak reverse current	Rated V_{RRM}	-	-	40	mA
I_{GKM}	Peak negative gate leakage current	V_{GR} = –16V	-	-	200	mA
V_{GT}	Gate trigger voltage	T_j = –40°C, V_D = 25V, R_L = 25mΩ	-	0.9	-	V
		T_j = 25°C, V_D = 25V, R_L = 25mΩ	-	0.8	-	V
		T_j = 125°C, V_D = 25V, R_L = 25mΩ	-	0.7	-	V
I_{GT}	Gate trigger current	T_j = –40°C, V_D = 25V, R_L = 25mΩ	-	1.5	6	A
		T_j = 25°C, V_D = 25V, R_L = 25mΩ	-	0.5	1	A
		T_j = 125°C, V_D = 25V, R_L = 25mΩ	-	125	400	mA
t_d	Delay time	(note 2)	-	0.8	-	µs
t_{gt}	Turn-on time	Conditions as for t_d, (10%I_{GM} to 10%V_D	-	3	5	µs
t_f	Fall time	(note 3)	-	0.8	-	µs
t_{gq}	Turn-off time	Conditions as for t_f, (10%I_{GQ} to 10%I_{TGQ}	-	10	11	µs
I_{GQ}	Turn-off gate current	Conditions as for t_f	-	190	-	A
Q_{GQ}	Turn-off gate charge		-	1.3	1.45	mC
t_{tail}	Tail time	Conditions as for t_f, (10%I_{TGQ} to I_{TGQ} < 1A	-	30	50	µs
t_{gw}	Gate off-time (note 4)	Conditions as for t_f	100	-	-	µs
R_{thJK}	Thermal resistance, junction to sink	Double side cooled	-	-	0.063	kW
		Cathode side cooled	-	-	0.21	kW
		Anode side cooled	-	-	0.09	kW
F	Mounting force	(note 5)	4.5	-	9.0	kN
W_t	Weight		-	120	-	g

note 1) Unless otherwise indicated T_j = 125°C

note 2) V_D = 50%V_{DRM}, I_{TGQ} = 700A, I_{GM} = 12A, di_G/dt = 6A/µs, T_j = 25°C, di/dt = 300A/µs, (10%I_{GM} to 90%V_D)

note 3) V_D = 50%V_{DRM}, I_{TGQ} = 700A, C_S = 1.5µF, di_G/dt = 20A/µs, V_{GR} = –16V, (90%I_{TGQ} to 10%I_{TGQ})

note 4) The gate off-time is the period during which the gate circuit is required to remain low impedance to allow for the passage of tail current.

note 5) For other clamping forces, consult factory.

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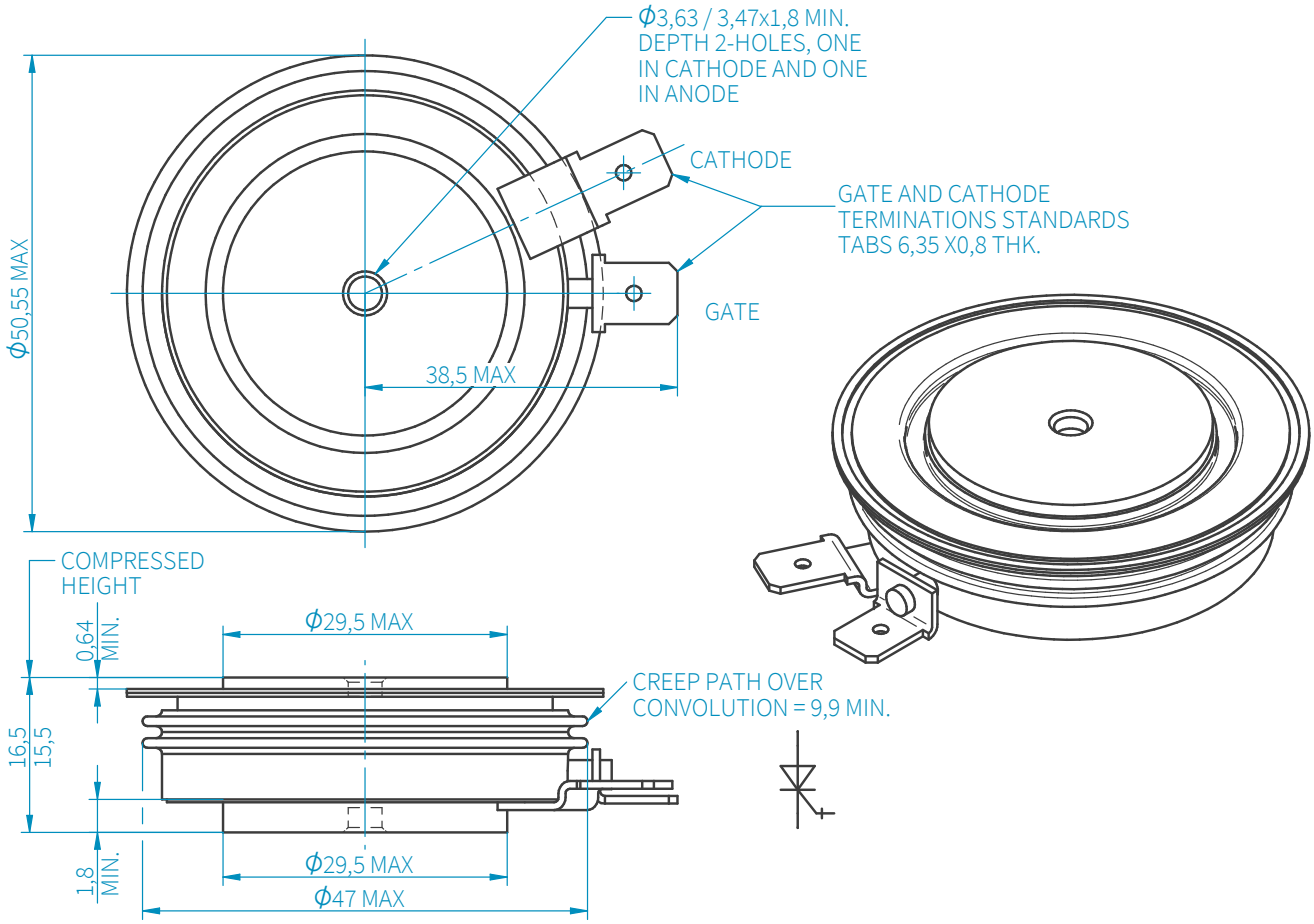
Outline Drawing



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