Distributed Gate Thyristor
Type SA21YP0878EK

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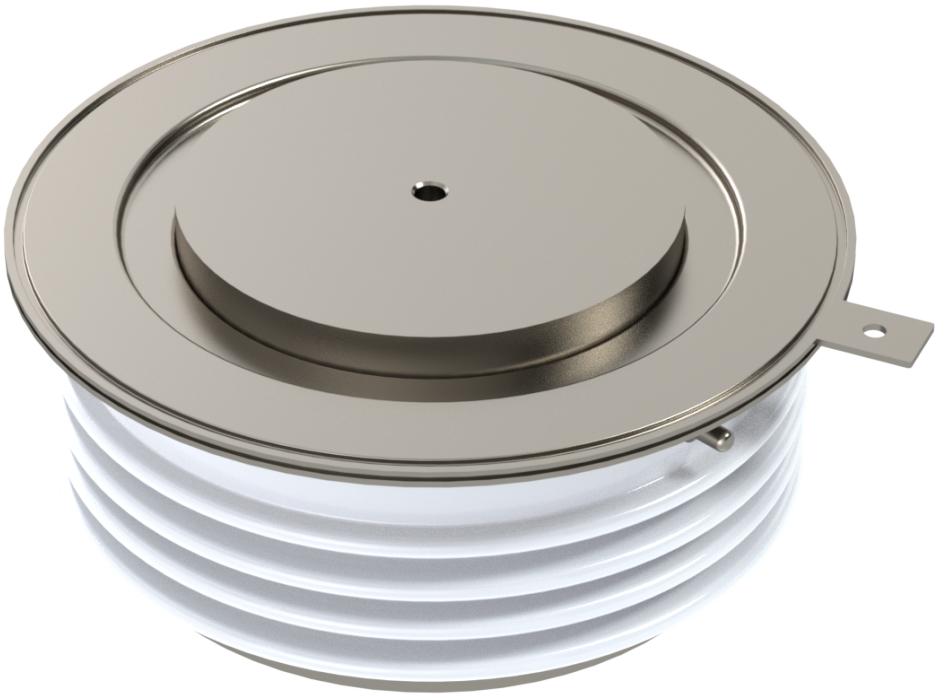

ORDERING INFORMATION						(Please quote 12 to 15 digit code as below)
SA	21	YP	0878	E	K	
-	Voltage Code	Outline Code	Current code	Type code	t_q code	Optional code
t_q code: K = 60µs, L = 65µs, M = 70µs						

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Absolute Maximum Ratings

	VOLTAGE RATINGS	MAXIMUM LIMITS	UNITS
V_{DRM}	Repetitive peak off-state voltage, (note 1)	2100	V
V_{DSM}	Non-repetitive peak off-state voltage, (note 1)	2100	V
V_{DDC}	Maximum DC of-state voltage, (note 1)	1300	V
V_{RRM}	Repetitive peak reverse voltage, (note 1)	1800	V
V_{RSM}	Non-repetitive peak reverse voltage, (note 1)	1900	V
V_{RDC}	Maximum DC revrese voltage, (note 1)	1150	V
note 1)	De-rating factor of 0.13%/°C is applicable for T_j below 25°C		

	OTHER RATINGS	MAXIMUM LIMITS	UNITS
$I_{T(AV)M}$	Maximum average on-state current, T_{sink} = 55°C, (note 1)	878	A
$I_{T(AV)M}$	Maximum average on-state current, T_{sink} = 85°C, (note 1)	583	A
$I_{T(AV)M}$	Maximum average on-state current, T_{sink} = 85°C, (note 2)	338	A
$I_{T(RMS)}$	Nominal RMS on-state current, T_{sink} = 25°C (note 1)	1765	A
$I_{T(d.c.)}$	D.C. on-state current, T_{sink} = 25°C, (note 3)	1456	A
I_{TSM}	Peak non-repetitive surge current t_p = 10ms, V_{RM} = 60%V_{RRM}, (note4)	7.50	kA
I_{TSM2}	Peak non-repetitive surge current t_p = 10ms, $V_{RM} \leq$ 10V, (note 4)	8.25	kA
I^2t	I^2t capacity for fusing t_p = 10ms, V_{RM} = 60%V_{RRM}, (note 4)	$281 \cdot 10^3$	A^2s
I^2t	I^2t capacity for fusing t_p = 10ms, $V_{RM} \leq$ 10V, (note 4)	$340 \cdot 10^3$	A^2s
$(di/dt)_{cr}$	Critical rate of rise of on-state current (repetitive), (note 5)	1000	A/µs
	Critical rate of rise of on-state current (non repetitive), (note 5)	1500	A/µs
V_{RGM}	Peak reverse gate voltage	5	V
$P_{G(AV)}$	Mean forward gate power	2	W
P_{GM}	Peak forward gate power	30	W
T_{jop}	Operating temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-40 to +150	°C
note 1)	Double-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 2)	Single-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 3)	Double-side cooled		
note 4)	Half-sinewave, 125°C T_j initial		
note 5)	V_D = 67%V_{DRM}, I_{FG} = 2A, $t_R \leq$ 0.5µs, T_{case} = 125°C		

Characteristics

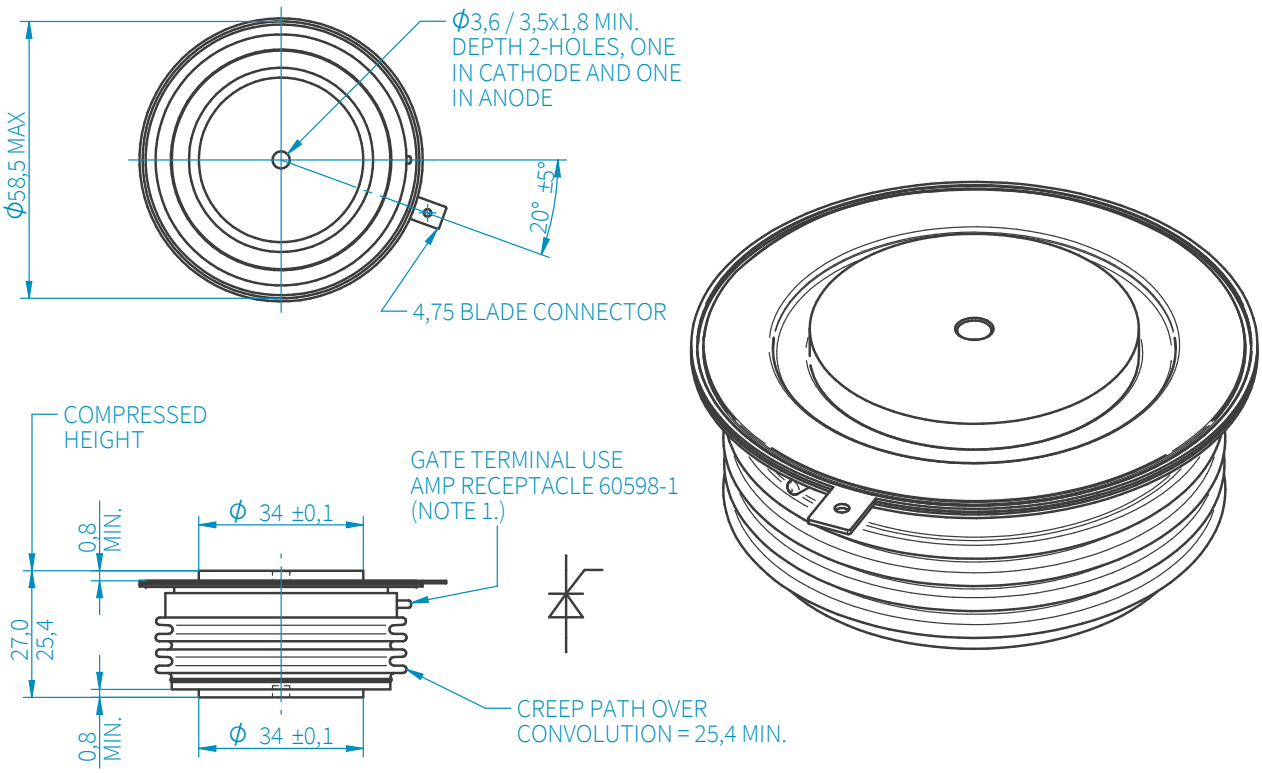
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{TM}	Maximum peak on-state voltage	I_{TM} = 1400A	-	-	2.12	V
		I_{TM} = 2650A	-	-	2.70	V
V_{T0}	Threshold voltage		-	-	1.447	V
r_T	Slope resistance		-	-	0.480	mΩ
$(dv/dt)_{CR}$	Critical rate of rise of off-state voltage	V_D = 80%V_{DRM}, Linear ramp, Gate o/c	200	-	-	V/µs
I_{DRM}	Peak off-state current	Rated V_{DRM}	-	-	70	mA
I_{RRM}	Peak reverse current	Rated V_{RRM}	-	-	70	mA
V_{GT}	Gate trigger voltage	T_j = 25°C, V_D = 10V, I_T = 3A	-	-	3.0	V
I_{GT}	Gate trigger current		-	-	300	mA
V_{GD}	Gate non-trigger voltage	Rated V_{DRM}	-	-	0.25	V
I_H	Holding current	T_j = 25°C	-	-	1000	mA
t_{GD}	Gate controlled turn-on delay time	V_D = 67%V_{DRM}, I_{TM} = 1500A, di/dt = 60A/µs, I_{FG} = 2A, t_r = 0.5µs, T_j = 25°C	-	0.8	2.0	µs
t_{GT}	Turn-on time		-	1.5	3.5	µs
Q_{RR}	Recovered charge	I_{TM} = 1000A, t_p = 1000µs,di/dt = 60A/µs, V_R = 50V	-	720	-	µC
Q_{RA}	Recovered charge, 50% Chord		-	350	400	µC
I_{RM}	Reverse recovery current		-	160	-	A
t_{RR}	Reverse recovery time		-	4.4	-	µs
t_{GQ}	Turn-off time (note 2)	I_{TM} = 1000A, t_p = 1000µs, di/dt = 60A/µs, V_R = 50V, V_{DR} = 80%V_{DRM}, dV_{DR}/dt = 20V/µs	-	-	65	µs
		I_{TM} = 1000A, t_p = 1000µs, di/dt = 60A/µs, V_R = 50V, V_{DR} = 80%V_{DRM}, dV_{DR}/dt = 200V/µs	60	-	70	µs
R_{thJK}	Thermal resistance, junction to sink (note 3)	Double-side cooled	-	-	0.032	K/W
		Single-side cooled	-	-	0.064	K/W
F	Mounting force	(note 3)	10	-	20	kN
W_t	Weight		-	340	-	g

note 1) Unless otherwise indicated T_j = 125°C

note 2) The required t_Q (specified with dV_{DR}/dt = 200V/µs) is 60µs

note 3) For other clamp forces, please consult factory

Outline Drawing



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