Phase Control Thyristor
Type SA24RR5715A0

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Date: October, 2020
Data Sheet Issue: 1

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SA	24	RR	5715	A	0	
-	Voltage Code	Outline Code	Current code	Type code	Special code	Optional code

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Absolute Maximum Ratings

	VOLTAGE RATINGS	MAXIMUM LIMITS	UNITS
V_{DRM}	Repetitive peak off-state voltage, (note 1)	2400	V
V_{DSM}	Non-repetitive peak off-state voltage, (note 1)	2400	V
V_{DDC}	Maximum DC of-state voltage, (note 1)	1450	V
V_{RRM}	Repetitive peak reverse voltage, (note 1)	2400	V
V_{RSM}	Non-repetitive peak reverse voltage, (note 1)	2500	V
V_{RDC}	Maximum DC revrese voltage, (note 1)	1450	V
note 1)	De-rating factor of 0.13%/°C is applicable for T_j below 25°C		

	OTHER RATINGS	MAXIMUM LIMITS	UNITS
$I_{T(AV)M}$	Maximum average on-state current, T_{sink} = 55°C, (note 1)	5715	A
$I_{T(AV)M}$	Maximum average on-state current, T_{sink} = 85°C, (note 1)	3975	A
$I_{T(AV)M}$	Maximum average on-state current, T_{sink} = 85°C, (note 2)	2315	A
$I_{T(RMS)M}$	Nominal RMS on-state current, T_{sink} = 25°C (note 1)	11200	A
$I_{T(d.c.)}$	D.C. on-state current, T_{sink} = 25°C, (note 3)	9910	A
I_{TSM}	Peak non-repetitive surge current t_p = 10ms, V_{RM} = 60%V_{RRM}, (note 4)	80	kA
I_{TSM2}	Peak non-repetitive surge current t_p = 10ms, $V_{RM} \leq$ 10V, (note 4)	88	kA
I^2t	I^2t capacity for fusing t_p = 10ms, V_{RM} = 60%V_{RRM}, (note 4)	$32.0 \cdot 10^6$	A^2s
I^2t	I^2t capacity for fusing t_p = 10ms, $V_{RM} \leq$ 10V, (note 4)	$38.7 \cdot 10^6$	A^2s
$(di/dt)_{cr}$	Critical rate of rise of on-state current (repetitive), (note 5)	150	A/µs
	Critical rate of rise of on-state current (non repetitive), (note 5)	300	A/µs
V_{RGM}	Peak reverse gate voltage	5	V
$P_{G(AV)}$	Mean forward gate power	5	W
P_{GM}	Peak forward gate power	30	W
T_{jop}	Operating temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-40 to +150	°C
note 1)	Double-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 2)	Single-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 3)	Double-side cooled		
note 4)	Half-sinewave, 125°C T_j initial		
note 5)	V_D = 67%V_{DRM}, I_{TM} = 4000A, I_{FG} = 2A, $t_R \leq$ 0.5µs, T_{case} = 125°C		

Characteristics

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{TM}	Maximum peak on-state voltage	I_{TM} = 6000A	-	-	1.35	V
V_{T0}	Threshold voltage		-	-	0.84	V
r_T	Slope resistance		-	-	0.085	mΩ
$(dv/dt)_{CR}$	Critical rate of rise of off-state voltage	V_D = 80%V_{DRM}, Linear ramp, gate o/c	1000	-	-	V/µs
I_{DRM}	Peak off-state current	Rated V_{DRM}	-	-	300	mA
I_{RRM}	Peak reverse current	Rated V_{RRM}	-	-	300	mA
V_{GT}	Gate trigger voltage	T_j = 25°C, V_D = 10V, I_T = 3A	-	-	3.0	V
I_{GT}	Gate trigger current		-	-	300	mA
V_{GD}	Gate non-trigger voltage	Rated V_{DRM}	-	-	0.25	V
I_H	Holding current	T_j = 25°C	-	-	1000	mA
t_{GD}	Gate controlled turn-on delay time	V_D = 67%V_{DRM}, I_{TM} = 2000A, di/dt = 10A/µs, I_{FG} = 2A, t_r = 0.5µs, T_j = 25°C	-	0.7	1.0	µs
t_{GT}	Turn-on time		-	1.2	3.0	µs
Q_{RR}	Recovered charge	I_{TM} = 3000A, t_p = 1000µs,di/dt = 10A/µs, V_R = 50V	-	8000	10500	µC
Q_{RA}	Recovered charge, 50% Chord		-	5460	-	µC
I_{RR}	Reverse recovery current		-	260	-	A
t_{RR}	Reverse recovery time, 50% Chord		-	42	-	µs
R_{thJK}	Thermal resistance, junction to sink	Double-side cooled	-	-	0.006	K/W
		Cathode-side cooled	-	-	0.013	K/W
		Anode-side cooled	-	-	0.012	K/W
F	Mounting force	(note 2)	76	-	93	kN
W_t	Weight		-	2000	-	g
note 1)	Unless otherwise indicated T_j = 125°C					
note 2)	For other clamp forces, please consult factory					

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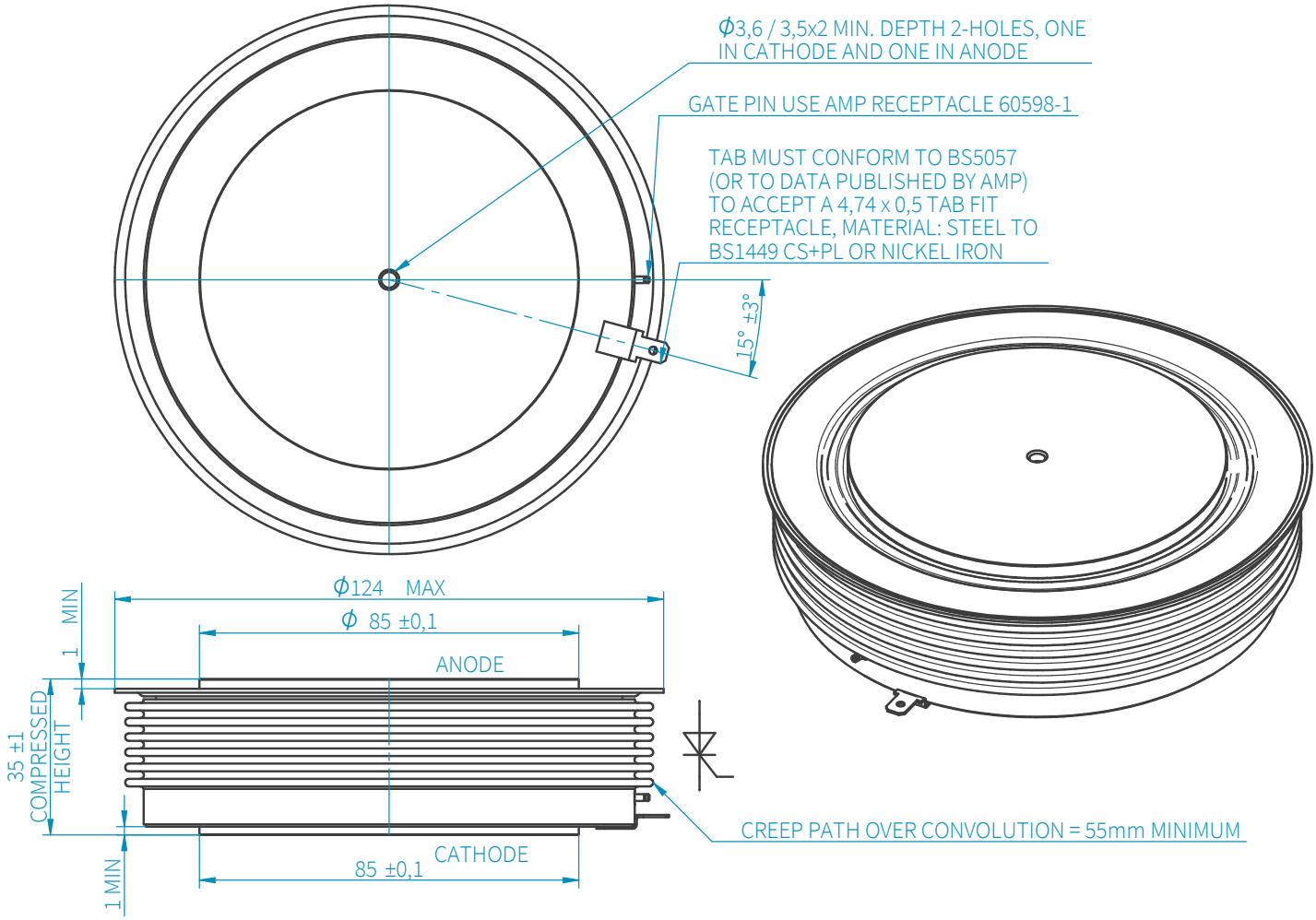
Outline Drawing



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