# Distributed Gate Thyristor Type SA42SN5145EW



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Date: September, 2020 Data Sheet Issue: 1



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SA	42	SN	5145	Е	W		
-	Voltage Code	Outline Code	Current code	Type code	t <sub>q</sub> code	Optional code	
$t_{q} \text{ code: } V = 250 \mu \text{s}, W = 300 \mu \text{s}$							

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#### **Absolute Maximum Ratings**

	VOLTAGE RATINGS	MAXIMUM LIMITS	UNITS
V <sub>DRM</sub>	Repetitive peak off-state voltage, (note 1)	4200	V
$V_{DSM}$	Non-repetitive peak off-state voltage, (note 1)	4300	V
$V_{DDC}$	Maximum DC of-state voltage, (note 1)	2500	V
$V_{RRM}$	Repetitive peak reverse voltage, (note 1)	4200	V
$V_{RSM}$	Non-repetitive peak reverse voltage, (note 1)	4300	V
$V_{RDC}$	Maximum DC revrese voltage, (note 1)	2500	V
note 1)	De-rating factor of 0.13%/°C is applicable for $T_j$ below 25°C		

	OTHER RATINGS	MAXIMUM LIMITS	UNITS
I <sub>T(AV)M</sub>	Maximum average on-state current, T <sub>sink</sub> = 55°C, (note 1)	5145	А
$I_{T(AV)M}$	Maximum average on-state current, T <sub>sink</sub> = 85°C, (note 1)	3450	А
$I_{T(AV)M}$	Maximum average on-state current, T <sub>sink</sub> = 85°C, (note 2)	1600	А
I <sub>T(RMS)</sub>	Nominal RMS on-state current, T <sub>sink</sub> = 25°C (note 1)	10290	А
I <sub>T(d.c.)</sub>	D.C. on-state current, T <sub>sink</sub> = 25°C, (note 3)	8610	А
I <sub>TSM</sub>	Peak non-repetitive surge current $t_p$ = 10ms, $V_{RM}$ = 60% $V_{RRM}$ , (note4)	66.0	kA
I <sub>TSM2</sub>	Peak non-repetitive surge current $t_p$ = 10ms, $V_{RM} \le$ 10V, (note 4)	72.5	kA
l <sup>2</sup> t	$I^2$ t capacity for fusing $t_p = 10$ ms, $V_{RM} = 60\%V_{RRM}$ , (note 4)	$21.78 \cdot 10^6$	$A^2s$
l <sup>2</sup> t	$\rm I^2t$ capacity for fusing $\rm t_p$ = 10ms, $\rm V_{RM} \le 10V$ , (note 4)	26.28 · 10 <sup>6</sup>	$A^2s$
(di/dt) <sub>cr</sub>	Critical rate of rise of on-state current (repetitive), (note 5)	500	A/µs
(ai/at/ <sub>Cr</sub>	Critical rate of rise of on-state current (non repetitive), (note 5)	1000	A/µs
$V_{RGM}$	Peak reverse gate voltage	5	V
$P_{G(AV)}$	Mean forward gate power	5	W
$P_{GM}$	Peak forward gate power	50	W
T <sub>jop</sub>	Operating temperature range	-40 to +125	°C
T <sub>stg</sub>	Storage temperature range	-40 to +150	°C
note 1)	Double-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 2)	Single-side cooled, single phase, 50Hz, 180° half-sinewave.		
note 3)	Double-side cooled		
note 4)	Half-sinewave, 125°C T <sub>j</sub> initial		
note 5)	$V_D$ = 67% $V_{DRM}$ , $I_{FG}$ = 2A, $t_R \le 0.5 \mu s$ , $T_{case}$ = 125°C		



#### **Characteristics**

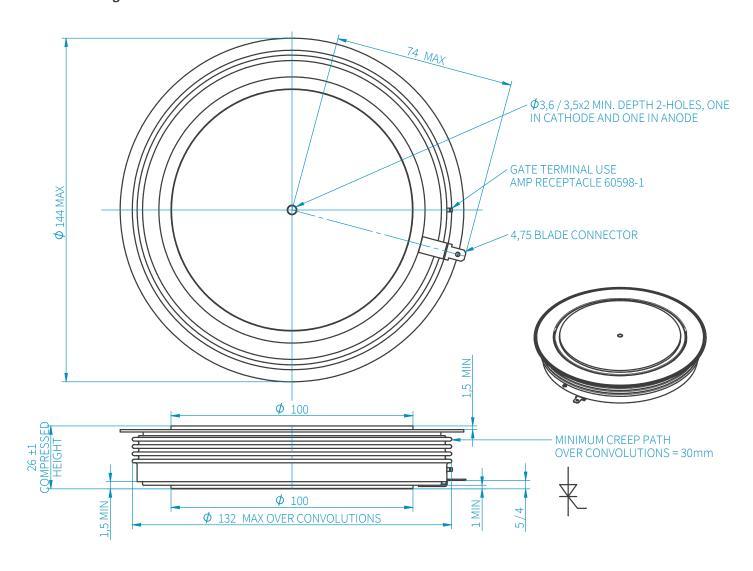
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{TM}$	Maximum peak on-state voltage	I <sub>TM</sub> = 6600A	-	-	2.35	V
$V_{T0}$	Threshold voltage		-	-	1.659	V
r <sub>T</sub>	Slope resistance		-	-	0.107	mΩ
(dv/dt) <sub>CR</sub>	Critical rate of rise of off-state voltage	V <sub>D</sub> = 80%V <sub>DRM</sub> , Linear ramp, Gate o/c	200	-	-	V/µs
I <sub>DRM</sub>	Peak off-state current	Rated V <sub>DRM</sub>	-	-	200	mA
I <sub>RRM</sub>	Peak reverse current Rated V <sub>RRM</sub>		-	-	200	mA
$V_{GT}$	Gate trigger voltage	T 2506 W 10W 24		-	3.0	V
$I_{GT}$	$T_j = 25^{\circ}\text{C}, V_D = 10\text{V}, I_T = 3\text{A}$ Gate trigger current		-	-	600	mA
$V_{GD}$	Gate non-trigger voltage Rated V <sub>DRM</sub>		-	-	0.25	V
I <sub>H</sub>	Holding current	T <sub>j</sub> = 25°C	-	-	1000	mA
$t_{\sf GD}$	Gate controlled turn-on delay time	$V_D = 67\%V_{DRM}, I_{TM} = 4000A, di/dt = 60A/\mu s,$ $I_{FG} = 2A, t_r = 0.5\mu s, T_j = 25^{\circ}C$		0.8	1.5	μs
t <sub>GT</sub>	Turn-on time			1.2	2.5	μs
$Q_{RR}$	Recovered charge		-	10500	12000	μC
$Q_{RA}$	Recovered charge, 50% Chord	$I_{TM} = 4000A$ , $t_p = 1000\mu s$ , $di/dt = 60A/\mu s$ ,		6200	-	μC
I <sub>RM</sub>	Reverse recovery current	$V_R = 50V$	-	750	-	А
t <sub>RR</sub>	Reverse recovery time			16.5	-	μs
		$I_{TM}$ = 4000A, $t_p$ = 2000 $\mu$ s, di/dt = 60A/ $\mu$ s, $V_R$ = 100V, $V_{DR}$ = 67% $V_{DRM}$ , d $V_{DR}$ /dt = 20V/ $\mu$ s	-	250	-	μs
$t_{GQ}$	Turn-off time (note 2)	$I_{TM} = 4000A$ , $t_p = 2000\mu s$ , $di/dt = 60A/\mu s$ , $V_R = 100V$ , $V_{DR} = 67\%V_{DRM}$ , $dV_{DR}/dt = 200V/\mu s$	-	300	-	μs
	Thermal resistance, junction to sink (note 3)	Double-side cooled	-	-	4.5	K/kW
$R_{\text{thJK}}$		Anode-side cooled	-	-	7.3	K/kW
		Cathode-side cooled	-	-	12.0	K/kW
F	Mounting force	(note 3)	80	-	100	kN
W <sub>t</sub>	Weight		-	2200	-	g
note 1)	Unless otherwise indicated T <sub>j</sub> = 125°C					
note 2)	The required $t_Q$ (specified with $dV_{DR}/dt = 200V/\mu s$ ) is $300\mu s$					
note 3)	For other clamp forces, please consult factory					

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